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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,773	07/17/2003	Kenneth B. Gilleo	CED 6005	1686

321 7590 02/10/2005

SENNIGER POWERS LEAVITT AND ROEDEL
ONE METROPOLITAN SQUARE
16TH FLOOR
ST LOUIS, MO 63102

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/621,773	GILLEO, KENNETH B.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *11-13,20-23 and 26-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,14-19,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/621773 Attorney's Docket #: CED 6005
Filing Date: 7/17/2003

Applicant: Gilleo

Examiner: Alexander Williams

Applicant's election of species I-IV (claims 1-10, 14-19, 24 and 25), filed 11/22/04, has been acknowledged.

This application contains claims 11-13, 20-23 and 26-28 drawn to an invention non-elected with traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 14-19, 24 and 25 are rejected under 35 U.S.C. § 102(b) as being anticipated byTsukagoshi et al. (U.S. Patent # 6.113.728).

US-PAT-NO: 6113728

(27) The present invention also provides a process for connecting circuits, comprising the steps of forming a filmy adhesive layer composed essentially of a liquid epoxy resin, a solid resin having a functional group and a micro-capsule type curing agent on the pressure-deformable projecting electrode-formed side of a semiconductor wafer formed with a plurality of integrated circuit elements having electrodes projecting from the main face; cutting said wafer along with the adhesive layer to form chips; positioning the projecting electrodes of said chips in register with the opposing circuits on a wiring substrate with said adhesive layer interposed therebetween; and substantially curing the adhesive after contacting the projecting electrodes with the opposing circuits by applying heat and pressure to said chips and wiring substrate.

1. Tsukagoshi et al. (figures 1 to 8) specifically figures 1c and 4 show an assembly comprising: a substrate, **3** an integrated circuit device **1** adapted to be electrically and mechanically connected to the substrate, electrical connection pads **2,4** on the integrated circuit device and on the substrate adapted to contact one another when the circuit device and the substrate are connected, said connection pads comprising at least one first projection **(see figure 4)** on one of the device and the substrate and at least two second projections on the other of the device and the substrate, each projection having a respective axial length extending from an external surface of a respective connection pad, the at least one first projection and at least two second projections having respective external surfaces that are sized and shaped for a close friction fit along their axial lengths when interdigitated relative to one another thereby to create an axial contact area between respective projections to establish an electrical and mechanical connection between the device and the substrate.

2. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said at least one first projection is on the integrated circuit device and said at least two second projections are on the substrate.
3. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said at least one first projection comprises a headless projection.

4. An assembler as set forth in claim 1, Tsukagoshi et al. show wherein said at least one first projection comprises a solid cylindrical body.
5. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said at least one first projection is substantially rigid.
6. An assembly as set forth in claim 4, Tsukagoshi et al. show wherein said body is formed integral with said one of the circuit device or substrate.
7. An assembly as set forth in claim 6, Tsukagoshi et al. show wherein said body comprises a metal external surface for contacting said at least two second projections.
8. An assembly as set forth in claim 4, Tsukagoshi et al. show wherein said at least two second projections comprise solid cylindrical bodies and are spaced apart to form an open space for receiving said at least one first projection.
9. An assembly as set forth in claim 8, Tsukagoshi et al. show wherein said solid cylindrical bodies of the first and second projections are substantially rigid.
10. An assembly as set forth in claim 8, Tsukagoshi et al. show wherein said second projections have metal external surfaces for contact with said body of the at least one first projection.

14. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said integrated circuit device is a MEMS device.

15. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said integrated circuit device is an optical MEMS device.

16. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said substrate is a chip carrier platform.

17. An assembly as set forth in claim 1, Tsukagoshi et al. show wherein said *substrate is a* circuit board.

18. Tsukagoshi et al. (figures 1 to 8) specifically figures 1c and 4 show a*n* assembly comprising: a substrate **3** having a plurality of connection pads **2,4**, each pad comprising *a* plurality of spaced apart electrically conductive substrate projections extending from an external surface of the pads and forming an open space therebetween, each substrate projection having a respective axial length, an integrated circuit device **1** adapted to be electrically *and* mechanically connected to the substrate, said device having a plurality of connection pads, each pad comprising at least one electrically conductive device projection extending from *an* external surface of the pad, each device projection having a respective axial length *and* being adapted for insertion into said open space such that the device and the substrate are held in electrical and mechanical connection by a friction fit between respective axial lengths of the substrate and device projections.

19. An assembly as set forth in claim 18, Tsukagoshi et al. show wherein at least one of said substrate and device projections comprises a solid cylindrical body having a metal external surface.

24. . Tsukagoshi et al. (figures 1 to 8) specifically figures 1c and 4 show an assembly comprising: a substrate **3**, an electrical circuit device **1** adapted to be electrically and mechanically connected to the substrate, a first connection pad **4** on the substrate comprising a first set of two or more electrically conductive connecting elements protruding from an external surface of one pad, each connecting element of the first set having an axial length generally perpendicular to the substrate,
a second connection pad **2** on the circuit device comprising a second set of one or more electrically conductive connecting elements protruding from an external surface of the pad and adapted for interdigitation with the connecting elements of the first set of connecting elements, each connecting element of the second set having an axial length, said first and second sets of connecting elements having respective external surfaces that are sized and **shaped for a** close friction fit along their axial length a when interdigitated relative to one another thereby to create an axial contact area between respective projections to establish an electrical and mechanical connection between said device axed the substrate.
25. An assembly as set forth in claim 24, Tsukagoshi et al. show wherein said second set of electrically conductive connecting elements **comprises a solid cylindrical body** having a metal external **surface**.

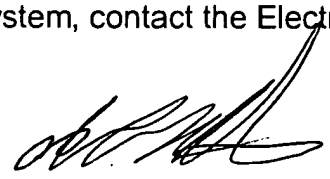
The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,738,737,734,698,691,692,693,678 156/264,281,305,306.9,330,264 29/832 174/259,255,260 361/760,773,779	2/7/05
Other Documentation: foreign patents and literature in 257/778,738,737,734,698,691,692,693,678 156/264,281,305,306.9,330,264 29/832 174/259,255,260 361/760,773,779	2/7/05
Electronic data base(s): U.S. Patents EAST	2/7/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
2/8/05